GaAs HBT Wideband Matrix Distributed and Darlington Feedback Amplifiers to 24 GHz

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Abstract—**This paper reports on the design and performance of a 2–24 GHz distributed matrix amplifier and a 1–20 GHz 2-stage Darlington coupled amplifier based on an advanced HBT MBE profile which increases the bandwidth response of the distributed and Darlington amplifiers by providing lower base-emitter and collector-base capacitances. The matrix amplifier has a 9.5 dB nominal gain and a 3-dB bandwidth to 24 GHz. This result benchmarks the highest bandwidth reported for an HBT distributed amplifier. The input and output VSWR's are less than 1.5:1 and 2.0:1, respectively. The total power consumed is less than 60 mW. The chip size measures 2.5×2.6 mm^2. The 2-stage Darlington amplifier has 7 dB gain and 3-dB bandwidth beyond 20 GHz. The input and output VSWR's are less than 1.5:1 and 2.3:1, respectively. This amplifier consumes 380 mW of power and has a chip size of 1.66×1.05 mm^2.**

I. Introduction

WIDEBAND HBT amplifiers have been reported earlier [1], [2] based on both distributed and Darlington feedback design approaches. HBT distributed amplifiers have achieved up to 10 GHz bandwidth [2] using a 3 μm self-aligned base ohmic metal (SABM) HBT technology. Single stage Darlington feedback amplifiers have achieved up to 20 GHz bandwidth [1] using 2 μm SABM HBT technology. The performance of HBT distributed amplifiers has been limited by the high base-emitter capacitance of the transistor. Bipolar devices in general, have an inherently high input capacitance, C_π, which depends on the base transit time, τ_B, of the device $[C_\pi = C_{je} + G_m(\tau_B + \tau_c)]$. Consequently, the high input capacitance limits the bandwidth that can be achieved by HBT distributed amplifiers. Device scaling and capacitive dividers at the input have been used for reducing the device input capacitance. The use of capacitive divider techniques alone is not an efficient solution for HBT devices since the high input capacitance of the device results in a large voltage division at the input of the device. Wideband bipolar feedback designs, on the other hand, are limited by the collector-base capacitance which is Miller multiplied by the voltage gain of the device. Device scaling and cascode configurations are design techniques that enhance the circuit frequency response. However, they do not address the transistor performance limitations which are related to the device design. An optimal solution will involve the implementation of both circuit techniques and device performance improvements.

This paper reports on the results of an HBT distributed amplifier and a Darlington feedback amplifier which use an advanced HBT MBE profile with an exponentially graded base doping [3] that creates a drift field component in the base resulting in a reduced base transit time, τ_B. The shorter transit time leads to a decrease in input capacitance as compared to the flat-doped (uniform) base profile. In addition, these designs are based on 2 μm emitter width devices. Consequently, the frequency bandwidth of the distributed amplifier has been extended from 10 GHz [2] to over 20 GHz. A 1 μm wide collector is also used to reduce the collector-base capacitance which is important for increasing the bandwidth of the Darlington feedback amplifier. With the aid of the reduced collector-base capacitance and a scaled-size input device in the Darlington cell, we have been able to implement a 2-stage Darlington amplifier that can achieve a 20 GHz bandwidth without excessive gain roll-off. Details of these results and a discussion of the design approaches are presented in the following sections.

II. GaAs HBT Technology

The GaAs HBT wideband distributed and Darlington-coupled amplifiers were fabricated using 2 μm SABM process technology. A cross section of the HBT integrated circuit process is shown in Fig. 1. This process integrates 2 μm emitter width npn HBT's, Schottky diodes, thin film resistors (NiCr), metal-insulator-metal (MIM) capacitors, and spiral inductors (air-bridged) facilitating monolithically combined microwave, analog, and digital functions. Details of this process and its applications have been reported elsewhere [4]. The HBT MBE profiles used in the fabrication of these amplifiers are illustrated in Fig. 2. The MBE profile incorporates an exponentially graded

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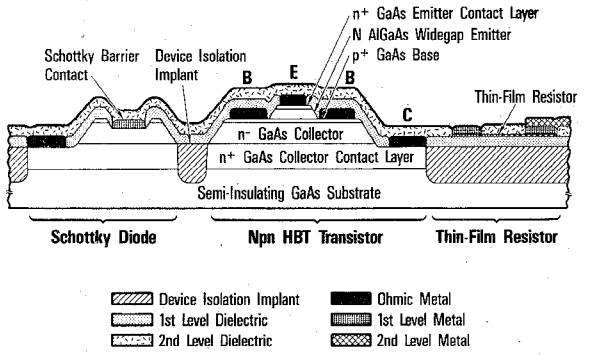

Fig. 1. Cross section of the GaAs HBT integrated circuit process technology.

base doping, from 5×10^{18} cm^{-3} at the collector to 5×10^{19} cm^{-3} at the emitter. The collector is 1.0 μm wide. The design of this novel profile and its measured effects on device performance have been reported earlier [3]. A SIMS profile of the graded structure is shown in Fig. 3. The base profile follows an exponentially decaying function from the emitter to the collector side of the base region which can be expressed as: $N_a(x) = N_o e^{-x/L}$ where $N_o = 5\times10^{19}$ cm^{-3} and $L = 608$ Å. For Be-doped Gallium Arsenide, carrier degeneracy occurs for doping concentrations approaching 5×10^{18} cm^{-3}. For state-of-the-art GaAs HBT technology, doping concentrations are on the order of 1×10^{19} cm^{-3} and greater. Thus the assumption of carrier non-degeneracy is no longer valid and the common statistical Boltzmann approximations for the carrier probability distribution can no longer be applied. Therefore, resultant E-field in the base region is given by

$$E = \frac{kT}{q}\cdot\frac{1}{Na}\cdot\frac{dNa}{dx} - \frac{kT}{q}\cdot\frac{dNa}{dx}\left[\frac{1}{Na} - \frac{1}{N_v F_{-1/2}(\eta_p)}\right]$$

where

$$\eta_p = \frac{E_v - E_f}{kT}.$$

The first term on the right hand side corresponds to the E-field assuming non-degenerate statistics. The second term is the correction in E-field when degeneracy is taken into account. This equation for the E-field can be further reduced to

$$E = \frac{1}{L}\cdot\frac{kT}{q}\left[\frac{Na}{N_v F_{-1/2}(\eta_p)}\right].$$

This equation includes a Fermi-function in the denominator and can be estimated using the Joyce–Dixon approximation [5]. The resultant E-field distribution in the base is found to be position dependent, where the distance is measured from the emitter edge of the base. This is different from the result of a constant E-field normally obtained for an exponentially graded doping profile assuming non-degeneracy. For the degenerate case derived above, the resultant field is calculated to be 1.33×10^4 V/cm at the emitter side and 5.296×10^3 V/cm at the collector side of the base region. The peak E-field at the emitter side of the base obtained for the degenerate case is about three times higher than the uniform field calculated using the non-degenerate statistics. The exponentially graded base profile which creates this drift field, however, also produces an opposing built-in field due to bandgap narrowing toward the base-emitter junction where the base is more heavily doped. The bandgap narrowing was measured to be 0.023 eV using optical techniques for Be-doped GaAs at room-temperature [6]. This corresponds to an opposing E-field of about 1.65×10^3 V/cm. The net peak E-field at the emitter edge of the base region, incorporating bandgap narrowing and the degeneracy assumption, is 1.165×10^4 V/cm. These quantitative calculations verify that the exponentially graded base profile can create a net E-field in spite of the opposing effects of bandgap narrowing in heavily p-type doped GaAs. Qualitatively, it may be inferred that there is an optimal solution which maximizes the net E-field produced in the base as a result of graded base doping in GaAs HBT's. The primary effect of this E-field is to sweep the electrons from the emitter to the collector edge of the base region, where otherwise, the only mechanism for electron transport is carrier diffusion. Thus, the built-in E-field reduces the base transit time and increases f_t.

The effect of the graded profile on f_t and f_{max} is compared to the uniformly doped profile (for a fixed collector width of 1.0 μm) in Fig. 4. The results indicate that the f_t has increased from 22 to 31 GHz and the f_{max} has increased from 40 to 58 GHz. The device f_t was measured at a practical current density of 20 kA/cm^2. For the exponentially graded base profile, f_{max} has increased due to a combination of higher f_t, lower series base resistance, R_b, and lower intrinsic collector-base capacitance, C_{bc}. The device f_{max} is given by

$$f_{max} = \left[\frac{f_t}{8\pi\cdot R_b\cdot C_{bc}}\right]^{1/2}.$$

The reduction in base resistance and collector-base capacitance has been verified by small signal modeling of S-parameters. Table I lists HBT small signal model parameters based on the equivalent circuit of Fig. 5 for three different MBE profiles. The profiles include a graded base doping with a 1 μm collector, a uniform base doping of 1×10^{19} cm^{-3} with a 1 μm collector, and a uniform base doping of 1×10^{19} cm^{-3} with a 0.7 μm collector. By comparing the model parameters of the three profiles, three conclusions concerning frequency response of the graded base device with the 1.0 μm collector can be deduced: 1) The input capacitance, $C\pi$, decreased by 25–30% due to a reduction in τ_B, 2) the collector-base capacitance significantly decreases from using a 1 μm wide collector, and 3) the base resistance has decreased because of the higher base doping (5×10^{19} cm^{-3}) on the emitter side of the graded base region.

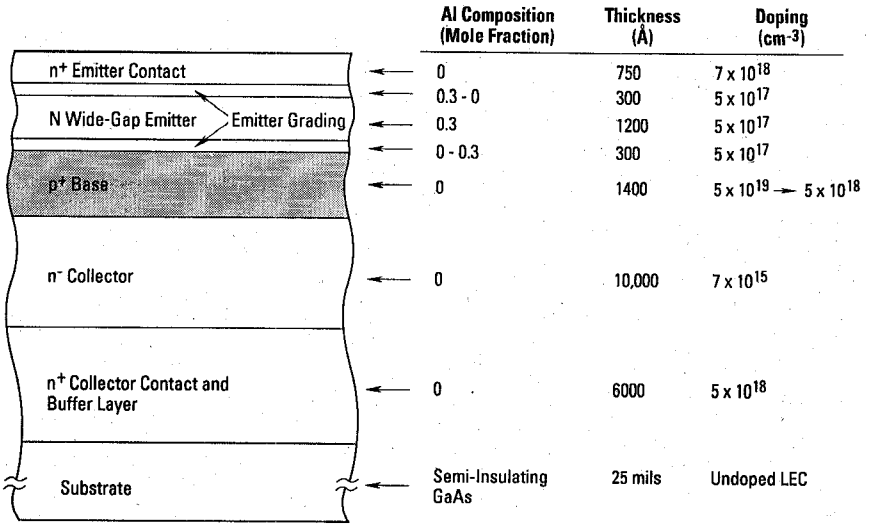

Fig. 2. GaAs HBT molecular beam epitaxy (MBE) cross section of the exponentially graded base profile.

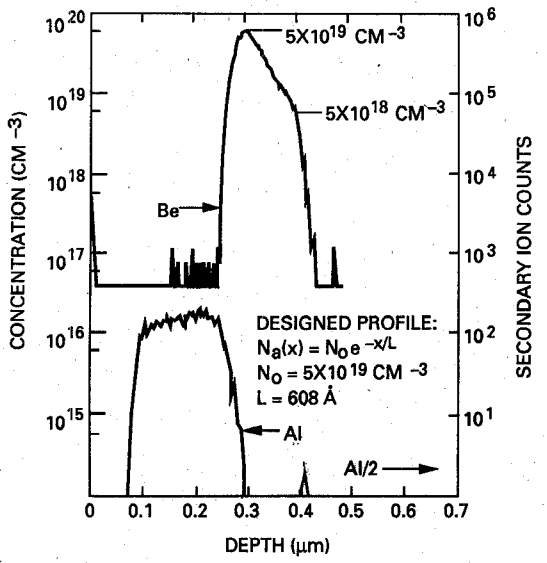

Fig. 3. SIMS of the exponentially graded base profile.

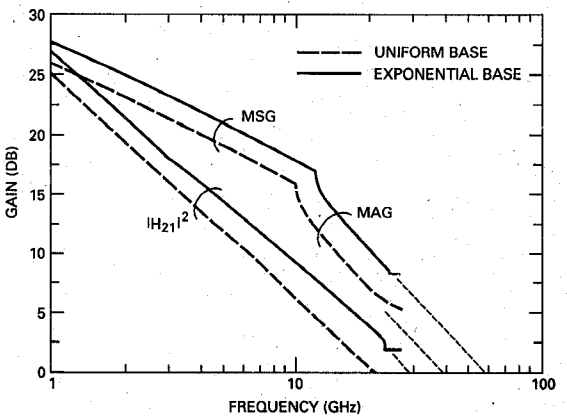

Fig. 4. Maximum stable/available gain and current gain (H21) vs. frequency for the uniform and exponentially graded base profiles.

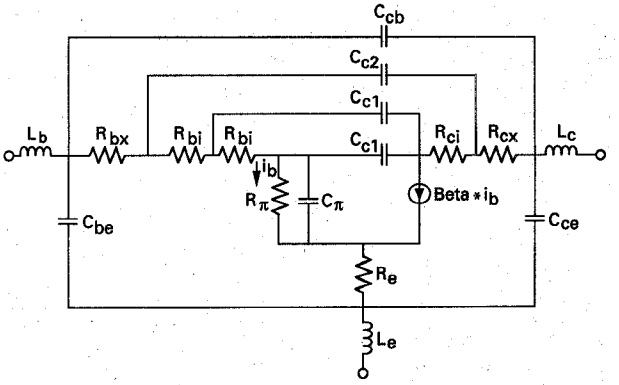

Fig. 5. HBT hybrid-π small signal equivalent circuit model.

These key features enhance the frequency response of the HBT distributed and feedback amplifiers.

III. Circuit Design and Performance

A. HBT Matrix Distributed Amplifier

Broadband microwave amplifier performance has been realized with GaAs MESFET and HEMT technologies using various design techniques. The most common approach to achieve broadband gain is to use a distributed or traveling-wave amplifier design topology which utilizes device parasitic parameters to construct artificial transmission lines coupled to the intrinsic device transconductance. The traveling wave concept goes back to its early use in vacuum tubes. It has been implemented for GaAs FET technologies and is well documented in literature [7]–[9]. Fig. 6 depicts the conventional distributed amplifier. In this topology the device transconductance couples the signal from the input transmission line to the output transmission line through each device section. The devices provide amplification of the signal so that there is overall gain through the system. Ideally, the traveling wave gets additively superimposed on the output transmission line at each section as it travels toward the output. The cut-off frequencies of the artificially synthesized input and output transmission lines limit the band-

TABLE I
HBT SMALL SIGNAL HYBRID-π MODEL PARAMETERS

MBE Profile		τ (ps)	R_π (Ω)	C_π (pf)	R_{bx} (Ω)	R_{bi} (Ω)	R_e (Ω)	C_{c1} (ff)	C_{c2} (ff)	R_{ci} (Ω)	R_{cx} (Ω)	C_{be} (ff)	C_{cb} (ff)	C_{ce} (ff)
Drift[1]	115	2.0	450	0.6	12	6	10	1.6	7.5	3	2	65	5	23
Flat Base[1]	70	2.6	400	0.85	15	10	12	4.0	7.0	3	2	70	8	23
Flat base[2]	58	2.95	416	0.81	12	17	13	3.6	14.0	2.2	2	60	4.5	28
								Intrinsic				Layout parasitics		

(1) Collector thickness 1.0 μm
(2) Collector thickness 0.7 μm

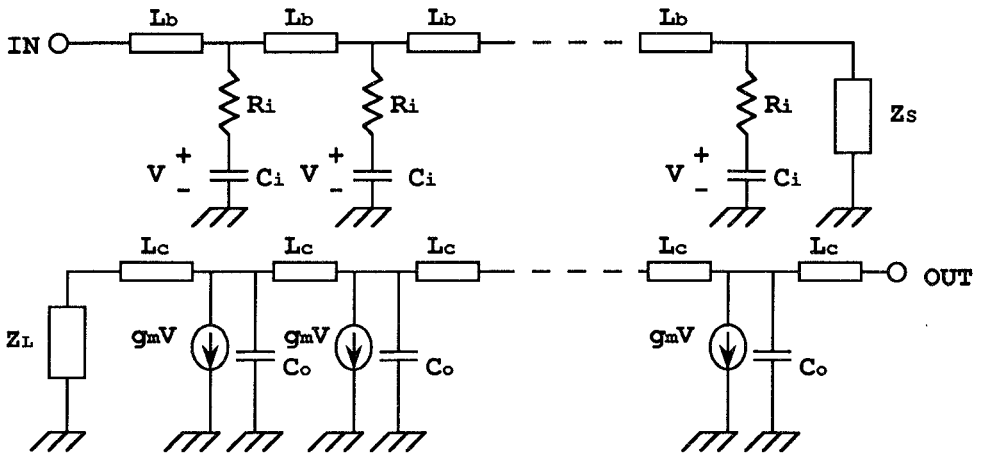

Fig. 6. Conventional distributed amplifier topology.

width. The cut-off frequencies are given by [9]

$$f_{ci} = \frac{1}{\pi\sqrt{L_b \cdot C_i}} \qquad f_{c.o} = \frac{1}{\pi\sqrt{L_b \cdot C_o}}.$$

For HBT's, as well as FET technologies, the input capacitance, C_i, creates the dominant cut-off pole for the distributed amplifier topology. The low input shunt capacitance, Cgs, and input gate resistance characteristic of the MESFET and HEMT technologies permit broadband distributed amplifier performance. HBT devices, on the other hand, have inherently higher input shunt capacitance, $C\pi$, which gives bipolar devices their characteristically higher transconductance. This limits the realization of wideband distributed amplifiers using HBT's. The high input capacitance is due to the close proximity of the base to the active conduction region when viewed as a charge controlled device [10]. This capacitance, C_π, consists of a base-emitter depletion capacitance and a diffusion capacitance component, $G_m(\tau_B + \tau_c)$. For microwave amplifiers, the transistor is usually biased at a collector current density where the diffusion capacitance is dominant. The diffusion capacitance is proportional to G_m:

$$G_m = \frac{I_c \cdot q}{kT}.$$

This relation shows that the diffusion capacitance term is dependent on collector bias current. The more power required from a device the higher the input capacitance. There is an obvious trade-off between power and bandwidth for an HBT distributed amplifier design. It is evident that by scaling the device size down, larger bandwidths can be achieved.

There are two common design techniques to reduce the input capacitance; 1) by using capacitive coupling [7], and 2) by device scaling. Since HBT's have inherently high input capacitance, the capacitive coupling technique results in a voltage division at the base input. In order to achieve a bandwidth of 20 GHz using a 2 μm$\times$10 μm quad-emitter device, this voltage division is about 1/6. This requires more device periphery to make up for the lost gain, however, it is effective in increasing the bandwidth. If the device is scaled down to a smaller size to get lower input shunt capacitance, the artificial transmission line must incorporate larger base and emitter resistances leading to a departure from an ideal lossless transmission line synthesis. This would degrade the gain-bandwidth product. The graded base profile extends the practical applicability of the two circuit techniques mentioned above, leading to a near optimal solution.

The matrix distributed amplifier topology was chosen [11], [12] instead of the conventional distributed amplifier topology. For HBT's, the matrix distributed topology offers more flexibility in using device scaling and capacitive coupling techniques. In this approach there are three coupled transmission lines where the intermediate transmission line is not constrained to a characteristic impedance of 50 Ω. This gives greater freedom in synthesizing the transmission lines to obtain the desired bandwidth.

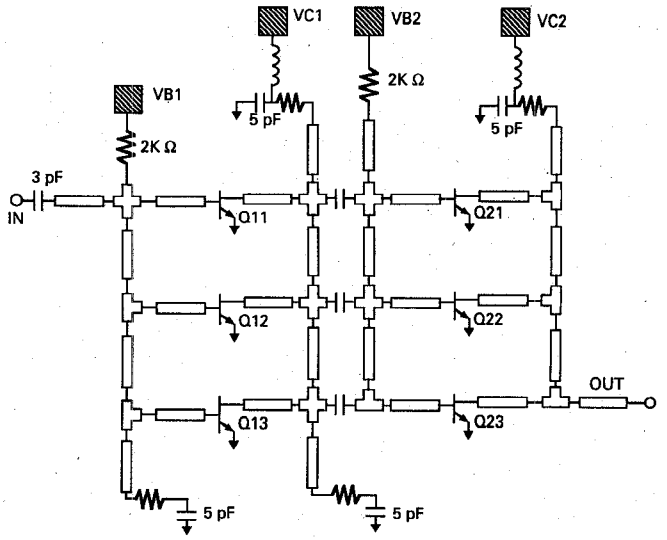

Fig. 7. Schematic diagram of the HBT distributed matrix amplifier.

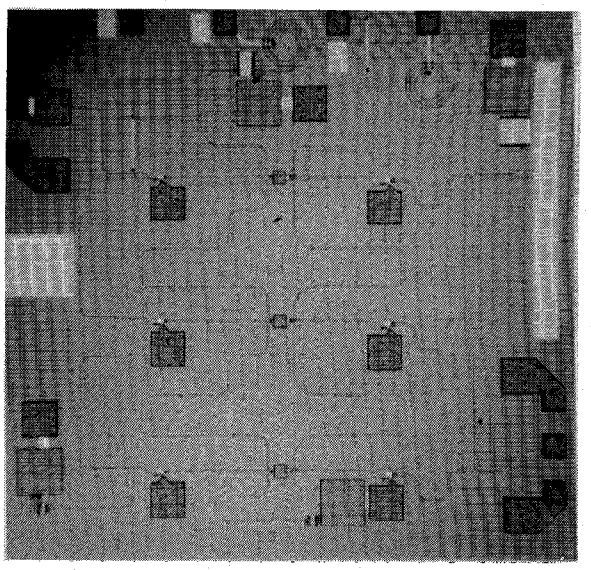

Fig. 8. Microphotograph of the HBT 2×3 matrix amplifier (chip size: 2.5×2.6 mm^2).

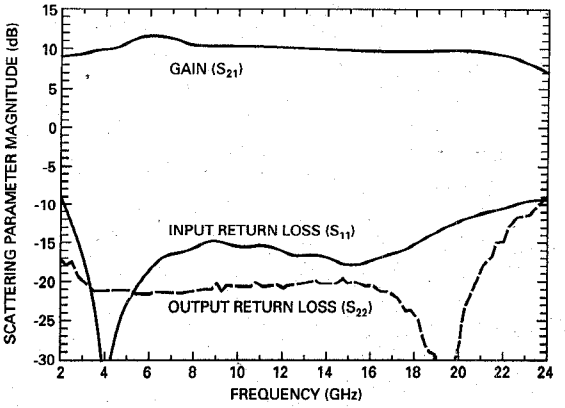

Fig. 9. Small signal performance of the HBT matrix distributed amplifier.

The schematic of the 2×3 matrix amplifier is presented in Fig. 7, which is similar to the MESFET matrix amplifiers mentioned earlier. The input row is realized by three 2 μm×6 μm single emitter devices which provide a suitable input capacitance required for a 20 GHz cut-off frequency. The output row is realized by three 2 μm×10 μm single emitter devices which are capacitively coupled to the input row of devices. The matrix amplifier is more flexible than the conventional distributed amplifier topology since the input row of devices can be scaled down to decrease the input capacitance while maintaining larger devices in the output row to obtain practical power. This scheme avoids capacitive coupling in the input row which reduces the power efficiency. Capacitive coupling is used between the input and output rows to increase the bandwidth. The line lengths and widths were constrained by symmetry for ease of layout. The chip was designed so that the base and collector of each row could be manually biased. All transistors are biased at a collector current density of 20 kA/cm^2. The fabricated 2×3 HBT matrix amplifier is shown in Fig. 8. The chip size is 2.5×2.6 mm^2. The wideband frequency response is shown in Fig. 9. The nominal gain is 9.5 dB with a 3-dB bandwidth to 24 GHz. The low-end gain response is flat down to 2 GHz where a 3 pF input coupling capacitance was chosen to roll off the gain. The measured input and output return loss illustrates excellent performance which is expected of distributed amplifiers. The input and output VSWR's are less than 1.5:1 and 2.0:1 from 2 to 20 GHz. Fig. 10 gives the noise figure performance over the frequency band. The noise figure is between 5.5–6.5 dB from 7 GHz to 18 GHz. From 7 GHz down to 2 GHz the noise figure increases linearly from 6 to 9.75 dB. This is believed to be caused by the small inter-stage coupling capacitors ($\approx$ 0.38 pF); they present a high impedance to the transistors of the 2nd stage at low frequencies which results in a noise mismatch. This explanation is supported by noise simulations of the circuit. The amplifier 1-dB compression was measured to be −2.5 dBm at midband. The input row of devices is biased at a $Vce = 1.5$ V and $Ic = 2.6$ mA. The output row of devices is biased at a $Vce = 2.0$ V and $Ic = 4$ mA. The total chip power dissipation is less than 60 mW.

B. Darlington Feedback Amplifier

Another topology, which is prominently used in high speed silicon and HBT bipolar technologies is the Darlington feedback amplifier. There are several previous experimental results given in literature on this amplifier [1], [13]–[15]. More recently, they have been introduced to HBT technology. The Darlington cell illustrated in Fig. 11 has many advantages for broadband realization of amplifiers. The primary advantage is that the Darlington cell can achieve twice the cut-off frequency of a single transistor. This cell is usually applied in a common emitter amplifier configuration. The low frequency voltage gain of a simple common emitter amplifier is proportional to the

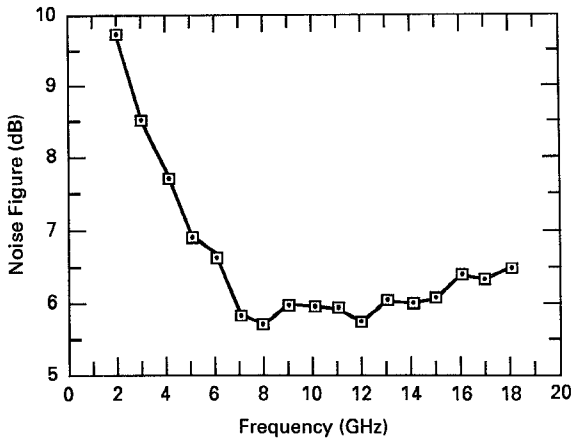

Fig. 10. Noise figure performance of the HBT matrix distributed amplifier.

ac beta of the transistor; $A_v \sim \beta_{ac}$. The low frequency ac beta, β_{ac}, of the transistor can be characterized by a dominant pole approximation given by

$$\beta_{ac}(s) = \frac{\beta_o}{1 + \frac{s}{\omega_\beta}}$$

where ω_β = the 3-dB frequency of the ac current gain. The 3-dB bandwidth, ω_β, of the current gain is related to the cut-off frequency of the device, $\omega_t = \beta_o * \omega_\beta$. This is derived by setting the magnitude of β_{ac} equal to unity. From the schematic of the Darlington cell, it can be shown that the effective ac current gain of the Darlington cell, β_{Deff}, is equal to $2\beta_{ac}$. This occurs when R_{bias} is adjusted such that the ac current in R_{bias} is equal to the ac current in the emitter of the output device. Under these conditions, the Darlington cell can have an effective cut-off frequency of $2\beta_o * \omega_\beta$ which is twice that of a single transistor. Consequently, the Darlington cell significantly improves the gain-bandwidth product of the common emitter amplifier topology. The implementation of the graded base profile which increases the f_t of the device, improves the bandwidth of the Darlington feedback amplifier. The primary device parameter which sets the dominant pole characteristics of the current and voltage gains for the Darlington amplifier, is the collector-base capacitance. By implementing a wide 1 μm collector MBE layer, the capacitance was significantly reduced. In addition, by scaling the input transistor of the Darlington cell to a smaller size a significant improvement in the bandwidth of the Darlington feedback amplifier has been achieved.

The schematic diagram of the 2-stage Darlington coupled HBT amplifier is shown in Fig. 12. The single stage consists of a Darlington amplifier which includes a 2 μm$\times$10 μm single emitter input transistor, followed by a 2 μm$\times$10 μm quad-emitter output transistor. The input and output transistors are biased at Ic = 3 mA and Ic = 12 mA respectively. The input transistor is scaled down to reduce power dissipation and also to improve the bandwidth as mentioned above. In addition, a series inductor-resistor load is used to reduce the required supply voltage. This resistor-inductor RF load also provides a low Q broadband gain peaking at the upper end. A microphotograph of the chip is shown in Fig. 13. The chip size is 1.66$\times$1.05 mm^2. The measured frequency response of the amplifier is shown in Fig. 14. The nominal gain is 7 dB with a 3-dB bandwidth of greater than 20 GHz. The 1 GHz low end roll-off is due to two 5 pF coupling capacitors. The input and output VSWR's are less than 1.5:1 and 2.3:1 over the frequency band, respectively. The noise figure performance, shown in Fig. 15, measures between 8 to 9.5 dB across the frequency band. The amplifier 1-dB compression was measured to be about 0 dBm at 10 GHz. The amplifier is self-biased and uses a 6 V supply. The total power consumed by the chip is 380 mW.

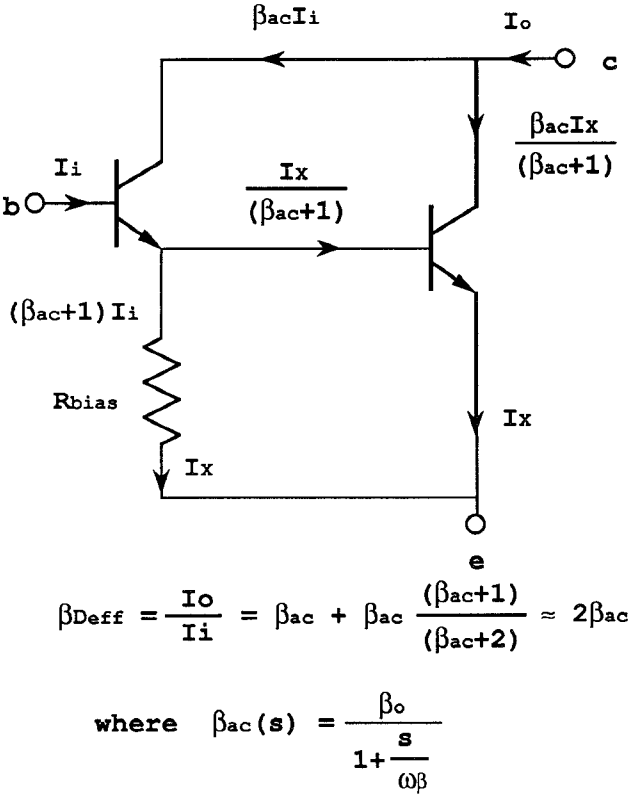

Fig. 11. Darlington amplifier cell.

IV. Summary

The design and performance of two different wideband amplifiers are presented. These amplifiers are based on an advanced exponentially graded base HBT MBE doping profile as well as circuit techniques to achieve broadband performance beyond 20 GHz. The implementation of the advanced MBE profile results in the improvement of HBT device characteristics which are crucial to the broadband performance of the matrix distributed amplifier and the Darlington feedback amplifier. The HBT matrix distributed amplifier achieves the widest bandwidth so far

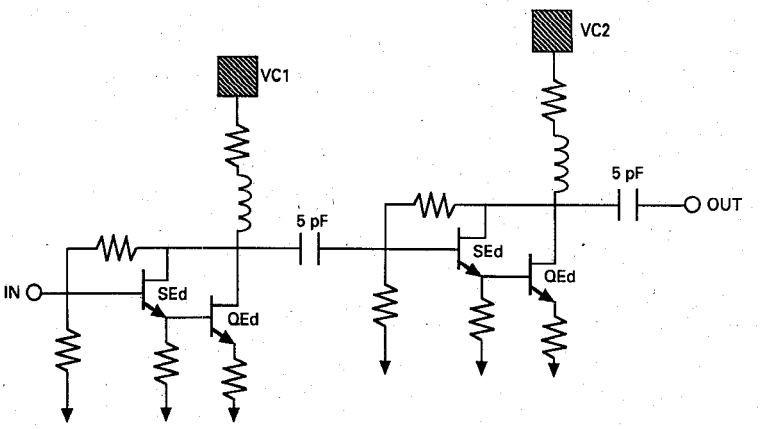

Fig. 12. Schematic diagram of the 2-stage Darlington feedback amplifier.

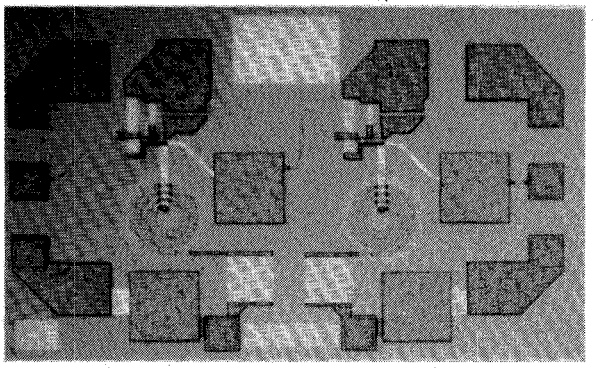

Fig. 13. Microphotograph of the fabricated 2-stage Darlington feedback amplifier chip size: 1.66×1.05 mm^2).

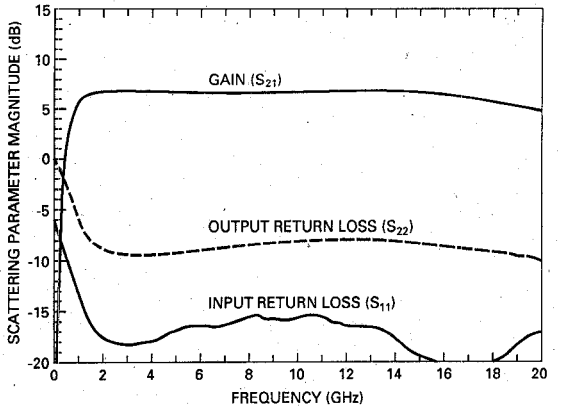

Fig. 14. Small signal performance of the 2-stage Darlington feedback amplifier.

reported for HBT distributed amplifiers and consumes less than 60 mW. The two stage HBT Darlington amplifier achieves a 1–20 GHz bandwidth which has matched the gain-bandwidth of a previously reported HBT single stage Darlington amplifier.

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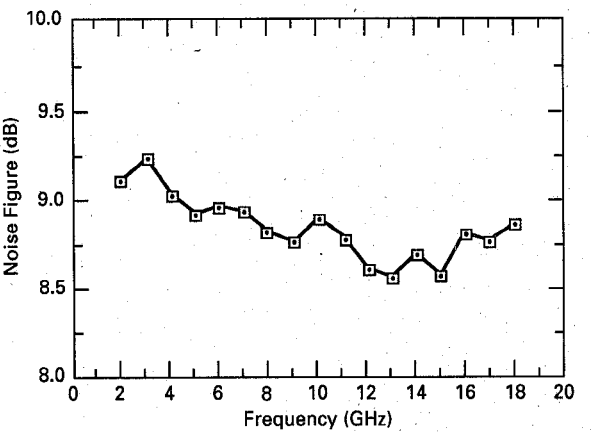

Fig. 15. Noise figure performance of the 2-stage Darlington feedback amplifier.

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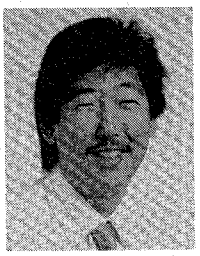
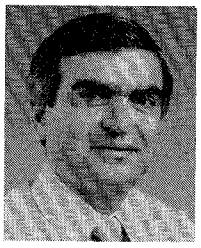


Kevin W. Kobayashi received the B.S.E.E. from the University of California at San Diego in 1986, and the M.S.E.E. from the University of Southern California in 1991.

Since 1986 he has been working at TRW's Advanced Microelectronics Laboratory in Redondo Beach, CA, where he has been involved in the development of GaAs HBT, MESFET and HEMT technologies. His primary focus is on HBT technology development which includes device characterization and modelling, device design, MMIC and analog circuit design. From 1985 to 1986 he was with Burroughs Microelectronics Group in the Device Physics Department, where he worked on the development of device/circuit simulation software and device modeling.



Reza Esfandiari (S'68–M'82–SM'90) received the B.S.E.E. and M.S.E.E. degrees from California State University-Sacramento in 1969 and 1970 respectively, and the Ph.D. degree from the University of California-Davis, in 1976.

Since 1985 he has been with TRW Electronics and Technology Division, where he has been engaged in the development of GaAs device and monolithic circuits technology. From 1979 to 1983 he was a Researcher Engineer at Hughes Aircraft Company Torrance Research Center. In 1983 he joined General Electric Company Electronic Laboratories. Previous to that he was with Zeta Laboratories in Santa Clara, CA and the Atomic Energy Organization of Iran Nuclear Research Center. He is currently managing the GaAs MANTECH program. Current interests are GaAs heterostructured devices, circuits and GaAs device reliability.

Dr. Esfandiari has been on the IEEE GaAs Integrated Circuit Symposium Technical Program Committee since 1986.

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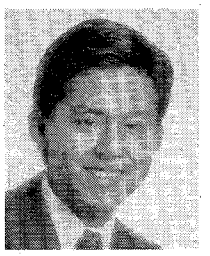
Since Jan. 1991 he has been with Hughes Research Laboratories, Malibu, CA, where he is involved with development of InP-based HBT and HEMT technologies in the Microwave Devices and Circuits Department. Prior to joining Hughes, he worked at TRW Inc., Redondo Beach, CA, for over five years, where he was a Senior Member of the Technical Staff in the Advanced Microelectronics Laboratory. His activities at TRW involved HBT and MESFET technology development including processing, device characterization and modeling, reliability studies, and circuit design. From 1983 to 1985 he worked at Signetics Corp., Sunnyvale, CA, on development of MOS EPROM and EEPROM technologies for nonvolatile memories. His current interests include device development, device physics, characterization and modeling, reliability studies, and circuit design.

Dwight C. Streit received the Ph.D. degree in electrical engineering from UCLA in 1986.

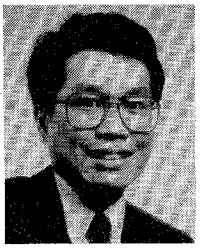
He is currently Manager of the GaAs Materials Section in TRW's Advanced Microelectronics Laboratory, where he is responsible for epitaxial material growth, ion implantation, and III-V material analysis. His primary research interest is the relationship between material characteristics and device performance. His work has dealt with both HBT and HEMT material development and device design.

Dr. Streit is a member of Tau Beta Pi, Eta Kappa Nu, and Sigma Xi. He is a 1991 recipient of the TRW Chairman's Award for Innovation.



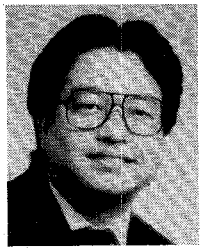
Aaron K. Oki (M'85) was born in Honolulu, Hawaii. He received the B.S. degree in electrical engineering in 1983 from the University of Hawaii, and the M.S. degree in electrical engineering and computer science in 1985 from the University of California, Berkeley.

After graduation he joined TRW as a member of the Technical Staff initiating HBT device and process development under Dr. M. E. Kim. He is actively involved in HBT characterization, modeling, processing, and circuit design. In 1990 he became the Principle Investigator for advanced HBT device and IC development and section head of the HBT product engineering section.



Liem T. Tran received the B.S. degree from California Institute of Technology, Pasadena, and the M.S. degree from University of California at Berkeley, all in electrical engineering.

He joined the Central Research Lab at Texas Instruments, Dallas, TX, in 1985, where he worked in the area of GaAs HBT for digital applications. Since 1988, he has been with the Advanced Microelectronics Lab at TRW, Redondo Beach, CA. His main interest involves HBT device processing and characterization for microwave, digital, and power applications.



Donald K. Umemoto (M'89) received the B.S. degree in biology in 1979 and the B.S and M.S. degrees in electrical engineering in 1986 and 1988, respectively, all from the University of Hawaii.

After obtaining the M.S. degree he joined TRW to work on GaAs HBT technology. He is now a Section Manager in the GaAs Advanced Microelectronics Laboratory. Mr. Umemoto is involved with the development of HBT, MESFET, and HEMT processing for microwave/millimeter wave, analog, digital, and A/D conversion applications.

Michael E. Kim (SM'90) received the B.S. and M.S. degrees in electrical engineering from the University of California, Los Angeles in 1972

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After his degree he spent an IBM postdoctoral year at M.I.T. and joined Rockwell International Science Center where he coordinated the development of HgCdTe monolithic infrared imaging devices and GaAs integrated optoelectronic circuits over a period of six years. In 1984 he joined TRW where he initiated the development of GaAs HBT IC technology and coordinated its application to advanced RF/analog, digital, and A/D conversion circuits over a period of six years. In 1991 he founded ADX MicroSys Corporation (Los Angeles), which is engaged in the development of next generation communications systems based on advanced microelectronics technologies.